EEDG6303 - Testing and Testable Design

EEDG 6303 (CE 6303) Testing and Testable Design (3 semester credit hours) Techniques for detection of failures in digital circuits and systems. Fault modeling and detection. Functional testing and algorithms for automatic test pattern generation (ATPG). Design of easily testable digital systems. Techniques for introducing built-in self test (BIST) capability. Test of various digital modules, such as PLA's, memory circuits, datapath, etc. Prerequisites: EE 3320 or equivalent and background in VHDL/Verilog. (3-0) Y