CE5325 - Hardware Modeling Using HDL

CE 5325 (EEDG 5325) Hardware Modeling Using HDL (3 semester credit hours) This course introduces students to hardware description languages (HDL) beginning with simple examples and describing tools and methodologies. It covers the language, dwelling on fundamental simulation concepts. Students are also exposed to the subset of HDL that may be used for synthesis of custom logic. HDL simulation and synthesis labs and projects are performed using commercial and/or academic VLSI CAD tools. Prerequisite: EE 3320 or equivalent. (3-0) T